REMARKS

Claims 1-33 were examined and reported in the Office Action. Claims 1-3, 9-11 and 28-33 are rejected. Claim 3 is cancelled. Claims 1-2, 4-16, 18-22 and 24-31 are amended. Claims 1-2 and 4-31 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §112, Second Paragraph

It is asserted in the Office Action that claims 9-17 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant has amended the claims to overcome the 35 U.S.C. §112, second paragraph rejections.

Accordingly, withdrawal of the 35 U.S.C. §112, second paragraph rejections for claims 9-17 are respectfully requested.

II. 35 U.S.C. § 102(b)

It is asserted in the Office Action that claims 1-3, 9-11, 28 and 31 are rejected under 35 U.S.C. § 102(b), as being anticipated by U. S. Patent No. 5,455,786 issued to Takeuchi et al ("Takeuchi"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2131, "'[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 1 contains the limitations of "[a] method for operating a non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells, each cell having a capacitor and a transistor having a floating gate, comprising: preparing a power-on mode for performing a DRAM operation; and preparing a power-off mode for storing data included in the capacitor into the floating gate."

Applicant's amended claim 28 contains the limitations of "[a] non-volatile dynamic random access memory (NVDRAM) device including a plurality of memory cells in a matrix, each memory cell comprising: a capacitor for storing data; and a transistor for transmitting the data stored in the capacitor to a bit line, wherein the transistor includes a drain, a source, and a gate having a control gate and a floating gate for storing the data when power is off, wherein one terminal of the capacitor is coupled to the drain of the transistor and another terminal of the capacitor is supplied with a controllable voltage determined according to an operation mode.

Applicant's amended claim 31 contains the limitations of "[a] non-volatile dynamic random access memory (NVDRAM) including a plurality of memory cells in a matrix, wherein each memory cell comprises: a control gate layer coupled to a word line; a capacitor for storing data; and a floating transistor for transmitting the stored data in the capacitor to a bit line and storing the data therein in response to an operation mode, wherein one terminal of the capacitor is coupled to a drain of the floating transistor and another terminal of the capacitor is supplied with a controllable voltage determined according to the operation mode."

Takeuchi discloses that data included in the ferroelectric capacitor remains in the ferroelectric capacitor as the polarization state of ferroelectric materials (see Takeuchi, column 1, lines 13-17). According to Applicant's claimed invention, however, data included in the capacitor is stored into the floating gate of the transistor during the power-off mode to save the data when power is off. Takeuchi does not teach, disclose or suggest "preparing a power-off mode for storing data included in the capacitor into the floating gate."

Moreover, Takeuchi does not teach, disclose or suggest connecting one terminal of the capacitor to a controllable voltage determined according to operational mode. That is, Takeuchi fails to disclose, teach or suggest "one terminal of the capacitor is coupled to the drain of the transistor and the other terminal of the capacitor is supplied with a controllable voltage determined according to an operation mode."

Therefore, since Takeuchi does not disclose, teach or suggest all of Applicant's amended claims 1, 28 and 31 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Takeuchi. Thus, Applicant's amended claims 1, 28 and 31 are not anticipated by Takeuchi. Additionally, the claims that directly or indirectly depend on claim 1, namely claims 2 and 9-11, are also not anticipated by Takeuchi for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 1-3, 9-11, 28 and 31 are respectfully requested.

III. 35 U.S.C. § 103(a)

A. It is asserted in the Office Action that claims 29-30 and 32-33 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Takeuchi in view of U.S. Patent Application No. 4,446,536 issued to Rodgers ("Rodgers"). Applicant respectfully traverses the aforementioned rejection for the following reasons.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the

prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's claims 29-30 either directly or indirectly depend on amended claim 28. Applicant's claims 32-33 either directly or indirectly depend on amended claim 31. Applicant has addressed Takeuchi regarding amended claims 28 and 31 above in section II.

Rodgers discloses an address drive circuit used for programmable, non-volatile semiconductor memories that use either Metal Nitrite Oxide Semiconductor (MNOS) or floating gate transistors for Electrically Erasable Programmable Read Only Memory Storage (EEPROMS). Rodgers, however, does not teach, disclose or suggest "one terminal of the capacitor is coupled to the drain of the transistor and another terminal of the capacitor is supplied with a controllable voltage determined according to an operation mode," or "one terminal of the capacitor is coupled to a drain of the floating transistor and another terminal of the capacitor is supplied with a controllable voltage determined according to the operation mode."

Therefore, even if Takeuchi were combined with Rodgers, the resulting invention would still not include all of Applicant's claimed limitations. And, therefore, there would be no motivation to combine Takeuchi with Rodgers. Thus, Applicant's amended claims 28 and 31 are not obvious over Takeuchi in view of Rodgers since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 28 and 31, namely claims 29 and 30, and 32 and 33, respectively, would also not be obvious over Takeuchi in view of Rodgers for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for claims 29-30 and 32-33 are respectfully requested.

IV. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 4-8 and 12-27 are objected to as being dependent upon a rejected base claim, but would

be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant respectfully asserts that claims 1-2 and 4-31, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-2 and 4-31 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: May 9, 2005

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on May 9, 2005.

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Jean Svoboda